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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/189,010	11/09/1998	TATSUYUKI TOKUNAGA	1232-4478	5014

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MORGAN & FINNEGAN, L.L.P.
3 WORLD FINANCIAL CENTER
NEW YORK, NY 10281-2101

EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/189,010	TOKUNAGA, TATSUYUKI	
	Examiner	Art Unit	
	Lin Ye	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-11 and 13-58* is/are pending in the application.

4a) Of the above claim(s) *4,5,15-17 and 23-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,3,6-11,13,14 and 18-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 November 1998* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 2/2/05 have been fully considered but they are not persuasive as to claims 2-3, 6-11, 13-14, 18-20 and 22.

For amended claims 2 and 14, the applicant argues that the Iwaski reference does not disclose, teach, or suggest "controlling charge accumulation... on the basis of the control information stored in said storage elements", because the elements 16 and 17 of the Iwaski reference does not to provide storing functionality. The examiner disagrees. The Iwaski reference discloses the both accumulation control circuits 16 and 17 **receiving** photometry information from the photometry region which was converted to digital signals by the A/D converter for **controlling the accumulation time** of the charge accumulation (See Iwaski reference. Col. 3, lines 40-55). For this reason, the accumulation control circuits 16 and 17 can be considered as the storage elements. It also should be noted that the Hirt reference discloses the Flash memory array 14 includes an array of individual memory locations for storing compensation values for controlling image signal levels accumulated by each pixel.

The applicant also argues that the Hirt reference does not disclose, teach or suggest that the programming signal controls photodiode accumulation operation. The examiner disagrees. The Hirt reference indicates the flash programmable memory 14 supplying the programming signal applied to the gate of the diver transistor 306 as shown in Figures 4-6 to control image signal levels accumulated by each pixel. It is well known in the art the image signal levels **proportional** to the product of light intensity and integration (accumulation)

time (e.g., the examiner cited the Hynecek U.S. Patent 6,229, 133 for evidence to support this statement; and please see Hynecek reference Col. 1, lines 20-24). For this reason, the programming signal controlling images signal levels also can be considered as controlling the charge accumulation time in the pixels.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-3, 6-11, 13-14, 18-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki U.S. Patent 5,497,215 in view of Hirt et al. U.S. Patent 5,883,830.

Referring to claim 2, the Iwasaki reference discloses in Figure 2, a photoelectric conversion device comprising: photoelectric converter (photometry part 10) including a plurality of photoelectric conversion elements (For example, photometry areas 10a and 10b) which is constructed by a plurality of pixels on a semiconductor substrate (See Col. 3, lines 15-24); and a plurality of storage elements (e.g., first accumulation control part 16 and second accumulation control part 17 store the photometry information from A/D converter 11 to controls the accumulation time of the photometry area 10a and 10b, see Col. 3, lines 40-48), each for storing predetermined control information employable in controlling

corresponding one of said photoelectric conversion element (e.g., the control part 16 control photometry area 10a, the control part 17 controls photometry area 10b); and a controller, wherein said controller controls charge accumulation of said photoelectric conversion converter (10a and 10b) on the basis of control information stored in said storage elements (16 and 17) (See Col. 3, lines 50-55). However, the Iwasaki reference does not explicitly states the plurality of storage means and photoelectric conversion means are formed on the same semiconductor substrate (single chip); and the storage elements includes a rewritable memory for control information.

The Hirt reference discloses in Figure 1, an single integrated chip (10) formed from a CMOS process on a single chip having an image sensor array (12), a flash programmable memory (14), a CPU (controller unit 16) and a interface circuit (A/D) including in the controller unit (See Col 4, lines 11-30 and Col. 5, lines 35-46). The flash programmable memory (14) has portions (reference numeral 24) for storing compensation and configuration values. The portions of memory (14) can be **rewritten** (reprogrammed, see Col. 5, lines 39) towards particular applications. For example, if the integrated circuit is intended for use within a video camera, then certain control information useful in such an application are stored within the memory (14). . It should be noted that the **configuration means** in the flash programmable memory (14) also includes the "**control means**" to control "charge accumulation of photoelectric conversion means", as shown in Figures 4-5 of Hirt reference, the controller circuit controls to transmit a flash programming signal (on the basis the information stored in the flash programmable memory 14) to a gate of drivel transistor 306 of photoelectric conversion means (12), thereafter, the multiplexed is controlled to transmit

output signals form the photodiode (e.g., the output signals form the photodiode is considered as the charge accumulated in the photoelectric conversion means, see Col. 7, lines 38-55; and It is well known in the art the image signal levels **proportional** to the product of light intensity and accumulation time. For this reason, the programming signal to control images signal levels also can be considered as control the charge accumulation time in the pixels) to provide automatic image compensation (See Col. 8, lines 4-7). The Hirt reference is an evidence that one of ordinary skill in the art at the time to see more advantages for integrating sensor, CPU and memory into a single chip, because it will significantly reduce the device size and making the device more portable; the storage means includes rewritable (reprogrammable) memory of control information for controlling an operation of the photoelectric conversion is rewritable by a predetermined program stored in a program memory so that a wide range of control information can be programmed to facilitate a wide range of applications (See Col. 6, lines 9-10) . For that reason, it would have been obvious to see said the plurality of storage elements and photoelectric conversion converter are formed on the same semiconductor substrate and the storage elements includes a rewritable memory for control information disclosed by Iwasaki.

Referring to claim 3, the Iwasaki reference discloses wherein said photoelectric conversion converter further includes a monitor (brightness calculator 12) for monitoring an accumulated charge state in said photoelectric conversion element, and said control means includes selector for selecting an arbitrary one of a plurality of pieces of status information (such as date and time and sets an initial accumulation time) on the basis of the control information stored in said storage means (16 and 17), and a comparator for comparing an

output from said monitor means with the status information selected by said selector, and controls the charge accumulation of said photoelectric conversion converter on the basis of comparison result of said comparator as shown in Figures 10-12 (See Col. 3, lines 40-55).

Referring to claim 6, the Iwasaki reference discloses a plurality of photoelectric conversion converter equivalent to said photoelectric conversion converter (10a and 10b).

Referring to claim 7, the Iwasaki reference discloses wherein said monitor monitors and outputs information based on a maximum accumulated charge amount of said photoelectric conversion element as shown in Figure 12 (See Col. 47-49).

Referring to claim 8, the Iwasaki reference discloses wherein said controller stores the status information selected by said selector in said storage means as the control information as shown in Figure 11.

Referring to claim 9, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 2.

Referring to claim 10, the Iwasaki reference discloses wherein said control means includes a circuit for determining predetermined information ion the basis of said output from said monitor, and stores the information determined by said determination means in said storage means as the control information as shown in Figure 10.

Referring to claim 11, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 10.

Referring to claim 13, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 3.

Referring to claim 14, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claims 2, 6 and 9.

Referring to claim 18, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 7.

Referring to claim 19, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 8.

Referring to claim 20, the Iwasaki and Hirt references disclose all subject matter as discussed with respected to same comment as with claim 10.

Referring to claim 22, the Iwasaki discloses the photometry system which computer-readably stores the processing steps of a control method as shown in Figure 10, steps S1-S6.

4. Claim 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki U.S. Patent 5,497,215 in view of Hirt et al. U.S. Patent 5,883,830 and Akashi et al. U.S. Patent 5,615,399.

Referring to claim 21, the Iwasaki and Hirt references disclose all subject matter as discussed in respected claim 2, except the references do not explicitly states a focus detection device including the photoelectric conversion device.

The Akashi reference disclose in Figure 1, the focus detecting apparatus including a photoelectric conversion device (area sensor 201). The Akashi reference is an evidence that one of ordinary skill in the art at the time to see more advantages for a focus detecting apparatus using an area sensor as an AF sensor, because the focus detecting device can be capable of accomplishing focus detection automatically and accurately. For that reason, it

would have been obvious to see said the focus detection device including the photoelectric conversion device disclosed by Iwasaki.

Conclusion

5. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Morris et al. U.S 6,665,010 discloses an imager includes groups of pixel sensing units and a control circuit.

   b. Hynecek U.S. 6,229,133 discloses the output image signal level is proportional to the integration time.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (571) 272-7372. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lin Ye
June 16, 2005

DAVID L. OMETZ
PRIMARY EXAMINER